

1. Overview

Features

Specified Operating Voltage Range:

- -Single supply voltage 4.5-5.5V
- -Functions up to 7.0V

Specified Operating Temperature Range:

-From -40C up to 150C

Linear Output with High Accuracy:

- -12-bit Ratiometric Rail-to-rail output
- -Digital Signal Processing

Magnetic Fields:

- -Static Fields and Dynamic Fields up to 2kHz
- -Ranges between -150mT to +150mT

EEPROM Parameters Adjustment

- -Magnetic range and SNST
- -Bandwidth setting
- -Polarity of output curve
- -Clamping option
- -Temperature coefficient for all common magnets
- -Memory Lock for Protection

Chip Protection:

- -Over Voltage and Under Voltage Detection
- -Open Circuit Detection

Supply Pulse Suppress

Programming:

- -2 wire programming interface
- -Re-programmable until Memory Lock
- -Individual Programming for Multiple Sensors Operation with the Same Supply and Ground

Calibration:

-2 Point Calibration

Industry standard SIP-4 Package

Applications

- -Contactless Potentiometers
- -Linear Position Sensing
- -Angular Position Sensing
- -Current Sensing
- -Magnetic Field Measurement

Product Description

MT1531 is a smart sensor providing an output voltage proportional to the magnetic flux through the hall plate and the supply voltage. It can be used for angle or distance measurements combined with a rotating or moving magnet.

MT1531 features a temperature-compensated Hall plate with chopper offset compensation, an A-to-D converter, digital signal processing, a D-to-A converter with output driver, an EEPROM memory with redundancy and lock function for the calibration data, a serial interface for programming the EEPROM, and protection devices at all pins.

MT1531 is fabricated in CZ6HFTSC, the 0.35um CMOS standard technology with embedded EEPROM and mixed-signal option devices.

Pin Configuration

Table 1-1: Pin Definition and Description

No	Pin	Function
1	VDD	Supply voltage / programming interface
2	GND	Ground
3	OUT	Output and selection pin
4	NC	No Connect

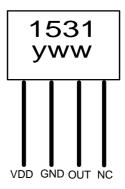


Figure 1-1: Pin definition on the package





2. General

2.1 Brief Theory of Operation

- -The magnetic flux is transferred to voltage signal by the Hall device
- -The output signal from the Hall device is converted to digital value through the ADC
- -Temperature compensation is processed by analog current bias
- -The output from ADC is processed by the DSP for range, gain and clamping, etc adjustment
- -The output from DSP is converted to analog value through the DAC
- -The output voltage is proportional to the supply voltage (ratiometric behavior)
- -Calibrate data is programmed to EEPROM by modulating the supply voltage

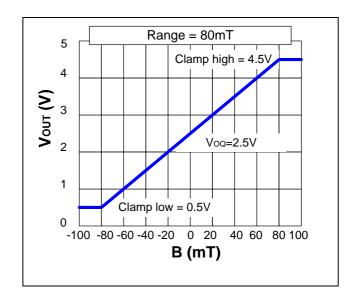


Figure 2-1: Example of Sensor Output

2.2 Transfer Function

Figure 2-1 shows one example of the chip operation.

2.3 Block Diagram

Figure 2-2 shows the simplified block structure.

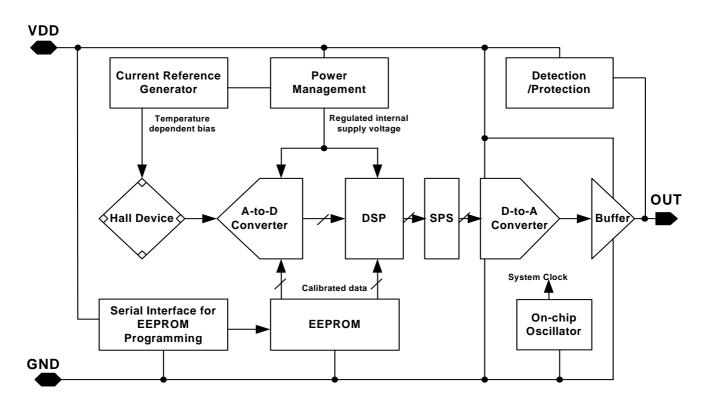


Figure 2-2: Block Diagram





3. Register Functions

3.1 DSP and Registers

The DSP plays a major role in the signal conditioning. The parameters for the DSP are stored in the EEPROM registers, shown in Figure 3-1.

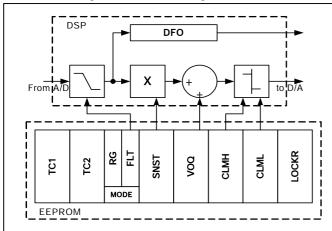


Figure 3-1: DSP and EEPROM customer registers

The EEPROM registers are divided into three groups.

Group 1 contains the registers for adjustment of the sensor to the magnetic system: MODE for selecting the magnetic field range and filter frequency, TC and TC2 for the temperature characteristics of the magnetic sensitivity.

Group 2 contains the registers for the defining the output characteristics: SNST, VOQ, CLML, and CLMH. The output characteristic of the sensor is defined by these four parameters: (See Figure 2-1 as an example)

- -The parameter VOQ (Output Quiescent Voltage) corresponds to the output voltage at B=0.
- -The parameter Sensitivity defines the magnetic gain.

$$Sensitivity = \frac{\Delta Vout}{\Delta R}$$

-The output voltage can be calculated as Vout ~ Sensitivity * B + Voq

The output voltage range can be clamped by setting the registers CLML and CLMH in order to enable failure detection (such as short-circuits to VDD or GND and open connections).

An external magnetic field generates a Hall voltage on the Hall plate. The ADC converts the amplified positive or negative voltage (operates with magnetic north and south poles at the branded side of the package) to a digital value. Positive values correspond to a magnetic north pole on the branded side of the package. The digital signal is filtered in the internal low pass filter and is readable in DFO register. During further processing, the digital signal is multiplied with the sensitivity factor, added to the quiescent output voltage and limited according to the clamping voltage. The result is finally converted to an analog signal.





3.2 Register Description

MODE

Shown in Figure 3-2 Mode register is divided into 2 parts: Filter and Range.

 MODE Register

 5
 4
 3
 2
 1
 0

 Filter
 Range

Figure 3-2: Mode register mapping

-Range: The Range bits define the magnetic field range of the sensor.

Table 3-1: Setting of Range bits

Range	Magnetic Field Range
0	-100 mT ~ 100 mT
1	-30 mT ~ 30 mT
2	-60 mT ~ 60 mT
3	-80 mT ~ 80 mT
4,5,6,7	-150 mT ~ 150 mT

-Filter: The Filter bits define the –3dB frequency of the digital low pass filter.

Table 3-2: Setting of Filter bits

Filter	-3dB Frequency
0	500 Hz
1	125 Hz
2	250 Hz
3	62.5 Hz
4	1 kHz
5, 6, 7	2 kHz

TC and TC2

The temperature dependence of the magnetic SNST can be adapted to different magnetic materials in order to compensate for the change of the magnetic strength with temperature. The adjustment is achieved by programming the TC (Temperature Coefficient) and TC2 (2nd order Temperature Coefficient) registers. The sensor can compensate for linear temperature coefficients ranging from – 3100 ppm/K up to 400 ppm/K and quadratic coefficients from about –5 ppm/K^2 to 5ppm/K^2.

DFO

This 14-bit register delivers the actual digital value of the applied magnetic field before the signal processing. This register can be read out and is the basis for the calibration procedure of the sensor in the system environment.

The DFO at any given magnetic field depends on the programmed magnetic field range but also on the filter frequency.

Table 3-3: DFO range

Filter Frequency	DFO Effective Range
62.5 Hz	-32,768 ~ 32,767
125 Hz	-32,768 ~ 32,767
250 Hz	-32,768 ~ 32,767
500 Hz	-32,768 ~ 32,767
1 kHz	-32,768 ~ 32,767
2 kHz	-32,768 ~ 32,767

SNST

The SNST register contains the parameter for the multiplier in the DSP. The SNST is programmable between –4 and 4. For VDD=5V, the register can be changed in steps of 0.00012. SNST=1 corresponds to an increase of the output voltage by VDD if the DFO increases by 65536.

For calculations, the digital value from the magnetic field of the ADC converter is used. This digital information is readable from the DFO register.

Sensitivity =
$$\frac{\Delta Vout * 65536}{\Delta DFO * VDD}$$

The register value is calculated by:

$$SNST = 8192 * Sensitivity$$

VOQ

The VOQ register contains the parameter for the adder in the DSP. Voq is programmed from –2VDD up to 2VDD. For VDD=5V, the register can be changed in steps of 0.305mV.

The register value is calculated by:

$$VOQ = 16384 * \frac{V_{OQ}}{VDD}$$



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For calibration in the system environment, a 2-point adjustment procedure is recommended. The suitable SNST and V_{QQ} values for each sensor can be calculated individually by this procedure.

CLML and CLMH

The CLML register contains the parameter for the lower limit. The lower clamping voltage is programmable between 0 \sim VDD. For VDD=5V, the register can be changed in steps of 0.610mV

The CLMH register contains the parameter for the upper limit. The upper clamping voltage is programmable between 0 ~ VDD. For VDD=5V, the register can be changed in steps of 0.610mV

The register value is calculated by:

CLML=8192*(Low Clamping Voltage)/VDD CLMH=8192*(High Clamping Voltage)/VDD

LOCKR

By setting this 8-bit register to 0B6H, all registers will be locked, and the sensor will no longer respond to any supply voltage modulation. This bit is active after the first power-off and power-on sequence after setting the LOCK byte.

3.3 Register List

Table 3-4: Customer register address

Register	Code	Bits	Format	Effective Range	Customer Operation	Notes
CLML	02~03H	13	Binary	0~8191	R/W/P	Low clamping voltage
CLMH	04~05H	13	Binary	0~8191	R/W/P	High clamping voltage
VOQ	06~07H	16	2's complement	-32768~32767	R/W/P	
SNST	08~09H	16	2's complement	-32768~32767	R/W/P	
MODE	0CH	6	Binary	0~63	R/W/P	Range and filter setting
LOCKR	01H	8	Binary	-	R/W/L	Lock bit
DFO	18~19H	16	2's complement	-32768~32767	R	
TC	0EH	8	Signed binary	-127~127	R/W/P	
TC2	0FH	6	Signed binary	-31~31	R/W/P	
TC3	10H	5	Signed binary	-15~15	R/W/P	

Note:

- 1. R=READ, W=WRITE, P=Program, and L=LOCK
- 2. There are special bit reverse exist in CLMH and SNST:

CLMH: every bit is reversed. For example, writing 00011110101 is actually 11100001010 for real calculations. SNST: only bit 13 is reversed. For example, writing 0000,0000,0000,0000 is actually 0010,0000,0000,0000 for real calculations (SNST=1).

VOQ: only bit 12 is reversed. For example, writing 0000,0000,0000,0000 is actually 0010,0000,0000,0000 for real calculations (VOQ=+0.5VDD)

Table 3-5: Reserved register address

Register	Code	Bits	Format	Range	Customer Operation	Notes
OFFS	0A~0BH	12	Binary	-2048~2047	-	
FOSCAD	17H	8	Binary	-128~127	-	
ID	00H	8	Binary	-	-	





4. Electrical and Magnetic Characteristics

4.1 Absolute Maximum Ratings

Absolute maximum ratings are limiting values to be applied individually, and beyond which the serviceability of the circuit may be impaired. Functional operability is not necessarily implied. Exposure to absolute maximum rating conditions for an extended period of time may affect device reliability.

Table 4-1: Absolute maximum ratings: all voltages listed are referenced to GND

Symbol	Parameters	Min	MAX	Unit	Notes
Ts	Storage temperature	-50	150	С	
TJ	Junction temperature	-50	170	С	
Тѕн	Output short circuit duration		10	min	
VDD	Supply voltage	-12.0	13.8	V	t < 1min, T _J < T _{JMAX}
IDDR	Reverse supply current		50	mA	TJ TJMAX
Vouт	Output voltage	-5.0	13.8	V	t < 1min, T _J < T _{JMAX}
Vout - VDD	Output voltage over VDD		2	V	
Іоит	Continuous output current	-10	10	mA	
Endurance	EEPROM programming cycles		200	Cycle	

4.2 Recommended Operating Conditions

Recommended operating conditions must not be exceeded in order to guarantee the performance of AM501.

Table 4-2: Recommended operating conditions

Symbol	Parameters	Min	TYP	MAX	Unit	Notes
TA	Ambient temperature	-40		150	С	
TJ	Junction temperature	-40		170	С	
VDD	Supply voltage	4.5	5.0	5.5	V	
Іоит	Continuous output current	-1.0		1.0	mA	
R∟	Output load resistance	4.5			Kohm	
CL	Output load capacitance	0.33	10	1000	nF	



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4.3 Electrical Characteristics

Table 4-3: Characteristics: at Ta=-40C to +150C, VDD=4.5 to 5.5V, after programming and locking, at Recommend Operation Conditions if not otherwise specified. Typical values for Ta=-25C and VDD=5V

Symbol	Parameters	Min	TYP	MAX	Unit	Conditions / Notes
Idd	Supply current		7	10	mA	
VDDZ	Over-voltage protection at VDD			14	V	IDD=25mA, TJ=25C, 20ms
Voz	Over-voltage protection at Output			14	V	Io=10mA, TJ=25C, 20ms
NRES	Number of bit for resolution		12		Bit	Ratiometric to VDD
DNL	DAC differential non-linearity	-1		1	LSB	
INL	Output integrated non-linearity	-0.5		0.5	%	Percentage of VDD
Er	Output ratiometric error in Vout/VDD	-0.5		0.5	%	Vout1-Vout2 >2V during calibration
	Output ratiometricy over temp. $\frac{V_{OUT}(VDD)}{VDD} / \frac{V_{OUT}(VDD = 5V)}{5V}$	99.5		100.5	%	Vout1-Vout2 >2V during calibration
Тк	Variation of linear temperature coefficient	-400		400	ppm/K	Suitable TC and TC2 for the application
Voutcl	Accuracy of output voltage at clamping low voltage	-45		45	mV	RL=4.7k , VDD=5V
Vоитсн	Accuracy of output voltage at clamping high voltage	-45		45	mV	RL=4.7k , VDD=5V
Vоитсн	Output high voltage	4.65	4.8		V	VDD=5V, Iout <1mA
Voutcl	Output low voltage		0.2	0.35	V	VDD=5V, Iout <1mA
FADC	ADC sampling frequency	-15%	320	+15%	kHz	
Tro	Output response time		16 8 4 2 1.5 1	32 16 8 4 3 2	ms ms ms ms ms	FFILTER = 62.5Hz FFILTER = 125Hz FFILTER = 250Hz FFILTER = 500Hz FFILTER = 1kHz FFILTER = 2kHz CL=10nF, BINPUT is stepped from 0 to BMAX and 10% to 90% of output is measured
TDO	Output delay time		0.1	0.5	ms	CL=10nF
Трод	Output settling time during power up time		24 12 6 3 2.5 2	40 20 10 5 4 3	ms ms ms ms ms	FFILTER = 62.5Hz FFILTER = 125Hz FFILTER = 250Hz FFILTER = 500Hz FFILTER = 1kHz FFILTER = 2kHz CL=10nF, settled to 90%
BW	Small signal bandwidth (-3dB)		2		kHz	Bac < 10mT, Ffilter=2kHz
Vnoise	Output noise (peak-to-peak)		3	6	mV	Range=100mT, FFILTER=62.5H SNST < 0.26 *2
Rоит	Output resistance		1	10	ohm	Voυτ is in range
RthJA	Thermal resistance junction to soldering point		150	200	C/W	

Note:



^{1.} More than 50% of the selected magnetic field range is used and the temperature compensation is suitable.

^{2.} Peak-to-peak value exceeded: 5%



4.4 Magnetic Characteristics

Table 4-4: Magnetic characteristics

Symbol	I Parameters Min TYP MA		MAX	Unit	Conditions / Notes	
Boffset Magnetic offset		-0.38	0	0.38	mT	B=0, Іоυт=0, Тл=25C
Boffset/ T	Magnetic offset versus TJ	-10	0	10	uT/K	В=0, Іоит=0

4.5 Detection Parameters

Table 4-5: Detection parameters: at Ta=-40C to +150C

Symbol	Parameters	Min	TYP	MAX	Unit	Conditions / Notes
Voutod	Output voltage at open VDD line	0		0.2	V	VDD=5V, RL=10k
Vouтog	Output voltage at open GND line	4.7		5.0	V	VDD=5V, RL=10k
VDDuv*1	Under-voltage detection level	3.8		4.4	V	
VDDov*1	Over-voltage detection level	8.5		10.0	V	

Note: 1.Over-voltage and under-voltage detection is enabled only after locking.

4.6 Spike Pulse Suppression (SPS) Parameters

Table 4-6: SPS parameters: at Ta=-40C to +150C

Symbol	Parameters	Min	TYP	MAX	Unit	Conditions / Notes
Tsp	Time of spike pulse			10	us	VDDmin > -2V
Trcr	Output recovery time after VDD OK			100	us	CL=100nF

In case of a short supply voltage interruption, the sensor will keep a record of the last measured value before the supply voltage interruption during reset procedure. See Figure 4-1 for the details.

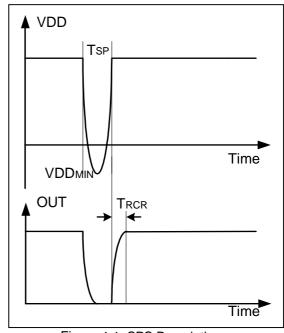


Figure 4-1: SPS Description





5. Application Information

5.1 Application Schematics

Figure 5-1 shows a typical application schematic using a single MT1531 sensor. Two capacitors (10~330nF) are recommended to connect between VDD to GND and OUT to GND respectively, to improve EMC.

Resistive load no less than 4.7k is permitted at OUTPUT.

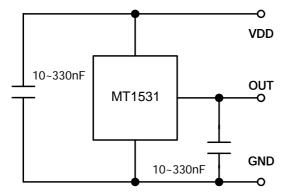


Figure 5-1: Recommended circuit for MT1531

5.2 Temperature Compensation

MT1531 features temperature compensation for 1st order and 2nd order coefficient covering almost all common magnets. Combinations of TC and TC2 are tabled for looking up.

Table 5-1: Frequently used settings: TBD



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5.3 Calibration

Recommended two-point adjustment for calibration is discussed.

Step 1: Input of the registers for general setting

The magnetic circuit, the magnetic material with its temperature characteristics, the filter frequency, and low and high clamping voltage are given for this application.

Therefore, the values of the following registers should be identical for all sensors of the customer application.

-FILTER

According to the maximum signal frequency -RANGE

According to the maximum magnetic field at the sensor position

-TC and TC2

Depends on the material of the magnet and the other temperature dependencies of the application -CLML and CLMH

According to the application requirements

Write the appropriate settings into the registers.

Step 2 Calculations of Voq and SNST

The calculation points 1 and 2 can be set inside the specified range. The corresponding values for VouT1 and VouT2 result from the application requirements.

Low clamping voltage VouT1,2 High clamping voltage

For highest accuracy of the sensor, calibration points near the minimum and maximum input signal are recommended. The difference of the output voltage between calibration point 1 and calibration point 2 should be more than 2.5V.

Set the system to calibration point 1 and read the register DFO. The result is the value DFO1.

Now, set the system to calibration point 2, read the register DFO again, and get the value DFO2.

With these values and the target values Vout1 and Vout2, for the calibration points 1 and 2, respectively, the values for SNST and Voq are calculated as:

$$Sensitivity = \frac{V_{OUT1} - V_{OUT2}}{DFO1 - DFO2} \cdot \frac{65536}{VDD}$$

$$V_{OQ} = V_{OUT1} - \frac{DFO1 \cdot Sensitivity \cdot VDD}{65536}$$

This calculation has to be done individually for each sensor.

Next, write the calculated values for SNST and VOQ into the chip for adjusting the sensor.

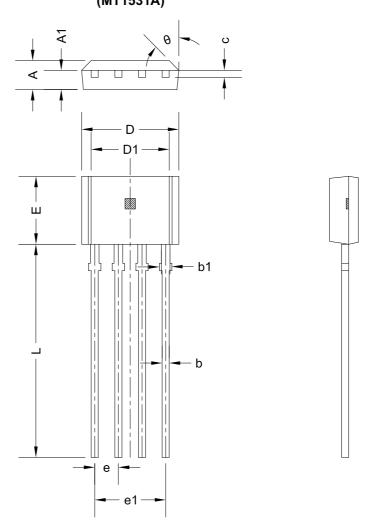
Step 3 Locking the Sensor

The last step is activating the LOCK function with the "LOCK" command. Please note that the LOCK function becomes effective after power-down and power-up of the Hall IC. The sensor is now locked and does not respond to any programming or reading commands.





PACKAGE DESIGNATOR (MT1531A)



Symbol	Dimensions in Millimeters		Dimensions in Inches	
	Min	Max	Min	Max
А	1.420	1.620	0.056	0.064
A1	0.660	0.860	0.026	0.034
b	0.350	0.480	0.014	0.019
b1	0.400	0.550	0.016	0.022
С	0.360	0.510	0.014	0.020
D	5.100	5.300	0.201	0.208
D1	4.100	4.300	0.161	0.169
Е	3.550	3.750	0.140	0.147
е	1.267	1.273	0.050	0.050
e1	3.780	3.840	0.149	0.151
L	13.600	15.500	0.535	0.610
θ	10°	12°	10°	12°

